RIO MEZZANINE CARD DESIGN GUIDE

# NI sbRIO-9607/9627

The NI sbRIO-9607 and sbRIO-9627 provide an embedded real-time processor, reconfigurable FPGA, and a RIO Mezzanine Card (RMC) connector. The RMC connector is a high-density, high-throughput connector that features 96 single-ended DIO lines directly connected to the FPGA with the ability to add up to two C Series modules and additional peripherals. Develop a custom RMC to integrate your own specific analog I/O, digital I/O, communication capabilities, and signal conditioning by combining these components onto a mating printed circuit board (PCB), known as an RMC.

In this document, the sbRIO-9607 and sbRIO-9627 are referred to inclusively as the sbRIO device.

This document provides detailed information about RMC design techniques, guidelines, and requirements.

**Note** Refer to the documents listed in the *Additional Documentation Resources* section of this chapter for more information as you design, prototype, and implement your sbRIO device application. In particular, refer to the *NI sbRIO-9607 User Manual* and *NI sbRIO-9627 User Manual* for dimensions and pinout information and the *NI sbRIO-9607 Specifications* and *NI sbRIO-9627 Specifications* for specifications for your sbRIO device.

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# Terminology

The following table defines terms used in this document to describe the sbRIO device concepts and technology.

**Table 1.** Terminology in This Document

| Term | Definition |
|---|---|
| System Components | |
| RMC connector | 240-pin, 40 × 6 position, high-density open pin field SEARAY on the sbRIO device. |
| SEARAY | Connector family used for the RMC connector on the sbRIO device. Manufactured by Samtec. |
| SoC | System on Chip. |
| USB Device | Physical, electrical, addressable, and logical entity that is attached to USB and performs a function. |

**Table 1.** Terminology in This Document (Continued)

| Term | Definition |
|---|---|
| USB Device port | Port on an RMC that provides a USB Device interface to the sbRIO device. |
| USB Host | USB interface that controls the bus and communicates with connected USB devices. |
| USB Host port | Port on an RMC that provides a USB Host interface from the sbRIO device. |
| Reference Schematic and Signal Naming | |
| LVTTL | In compliance with the Low-Voltage Transistor-Transistor Logic (LVTTL) specification. |
| LVCMOS | In compliance with the Low-Voltage Complementary Metal Oxide Semiconductor (LVCMOS) specification. |

# Schematic Conventions

The following table describes symbol conventions used in the I/O interface schematic diagrams in this document.

**Table 2.** Schematic Conventions in This Document

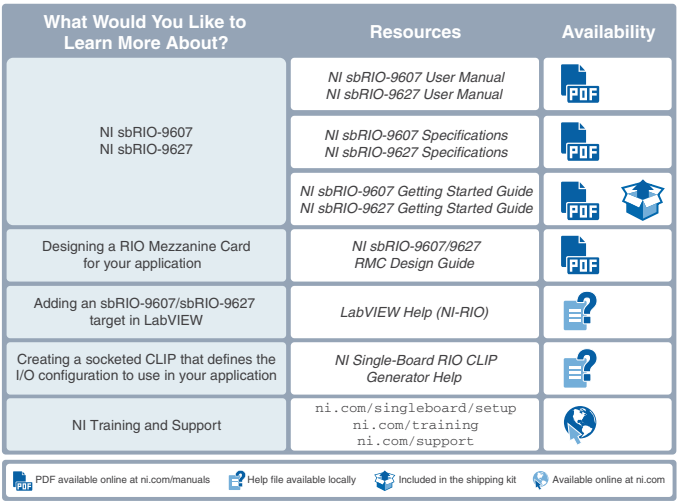
| Symbol | Description |
|---|---|
| | Off-page symbol that represents communication to and from the mating connector. |
| | Off-page symbol that represents communication from the mating connector. |
| | Off-page symbol that represents communication to the mating connector. |
|  | On-page symbol that represents the signal being driven. |
|  | On-page symbol that represents the signal being received. |
| | Power supply rail. |
| | Analog ground. |
| | Digital ground. |

**Table 2.** Schematic Conventions in This Document (Continued)

| Symbol | Description |
|---|---|
| | Chassis ground. |
| SPARE | Refers to an unpopulated reference designator. |

# Additional Documentation Resources

Refer to the following additional resources as you design, prototype, and implement your sbRIO device application.


What Would You Like to Learn More About?
Resources
Availability
NI sbRIO-9607
NI sbRIO-9627
NI sbRIO-9607 User Manual
NI sbRIO-9627 User Manual
NI sbRIO-9607 Specifications
NI sbRIO-9627 Specifications
NI sbRIO-9607 Getting Started Guide
NI sbRIO-9627 Getting Started Guide
Designing a RIO Mezzanine Card for your application
NI sbRIO-9607/9627 RMC Design Guide
Adding an sbRIO-9607/sbRIO-9627 target in LabVIEW
LabVIEW Help (NI-RIO)
Creating a socketed CLIP that defines the I/O configuration to use in your application
NI Single-Board RIO CLIP Generator Help
NI Training and Support
ni.com/singleboard/setup
ni.com/training
ni.com/support
PDF available online at ni.com/manuals
Help file available locally
Included in the shipping kit
Available online at ni.com

# Design Recommendations for Compatibility

Use the following table to determine if a previously designed RMC is compatible with the new RMC pinout and as guidance on how to design an RMC for compatibility with future generations of the RMC.

**Table 3.** RMC Connector Feature Set Compatibility

| Feature Set | sbRIO-9605/06/23/26 | sbRIO-9607 and sbRIO-9627 | Future Design Compatibility |
|---|---|---|---|
| DIO[0..63] | Yes | Yes | Yes |
| DIO[64..95] | Yes | Yes | Not guaranteed |
| FPGA_CONF | Yes | Yes | Yes |
| USB_D+/- | Yes | Yes | Yes |
| RST# | Yes | Yes | Yes |
| SYS_RST# | Yes | Yes | Yes |
| 5V | Yes | Yes | Yes |
| 3.3V_AUX | Yes | Yes | Yes |
| FPGA_VIO | Yes | Yes | Yes |
| PROC_VIO | Yes | No[1] | Not guaranteed |
| VBAT | Yes | Yes | Yes |
| GP_PORT<br>CAN<br>RS-232<br>RS-485<br>Secondary Ethernet<br>SDHC | Yes | No | Not guaranteed |
| Processor I/O via DIO[0..95]<br>CAN<br>RS-232<br>RS-485<br>SDHC | No | Yes | Not guaranteed |
| GBE_MDI[0..3+/-] | No | Yes | Not guaranteed |

[1] Pin 42 - RESERVED of the RMC connector provides 3.3 V to the RMC in order to maintain compatibility with the sbRIO-9605/06/23/26 RMC pinout. This pin is not recommended for use with new designs.

**Table 3.** RMC Connector Feature Set Compatibility (Continued)

| Feature Set | sbRIO-9605/06/23/26 | sbRIO-9607 and sbRIO-9627 | Future Design Compatibility |
|---|---|---|---|
| USB_MODE, USB_CPEN, USB_VBUS | No | Yes | Not guaranteed |
| Dedicated C Series DIO | No[2] | Yes | Not guaranteed |
| VIN_FILTERED | No | Yes | Yes |

# Fixed Behavior Signals

A subset of pins on the RMC connector on the sbRIO device are dedicated to implementing the following specific I/O functionality:

- Power rails
- Gigabit Ethernet (GBE)
- USB Host/Device (USB)
- C Series (SLOT 1, SLOT 2)

Other pins on the RMC connector are dedicated to implementing the following support signals:

- RTC Battery (VBAT)
- Resets
- Status LED
- FPGA Config

**Note** Refer to the *NI sbRIO-9607 User Manual* or *NI sbRIO-9627 User Manual* for a complete list of all pins and signals on the RMC connector.

Refer to the specific sections in this document for more information about how the RMC implements each signal.

## Power Rails

The sbRIO device provides the following power rails for use on an RMC:

[2] The sbRIO-9605/06/23/26 supports C Series I/O using the NI 9693 RMC.

**Table 4.** Power Rails

| Power Rail | Signal Name |
|---|---|
| Secondary Power Input | VIN_Filtered |
| Power Output | 3.3V_AUX<br>FPGA_VIO<br>5V<br>5V C Series |

## Power Rails Signal Definitions

The following table describes the power rails pins and signals on the sbRIO device connector.

**Table 5.** Power Rails Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| 3.3V_AUX | 48 | O | — | 3.3 V_AUX from the RMC connector host system. The rail is always on when the main host system is connected to power. |
| FPGA_VIO | 234<br>240 | O | — | I/O voltage for the FPGA 3.3 V pins. |
| 5V | 54<br>60<br>66<br>72 | O | — | 5 V from the RMC connector host system. |

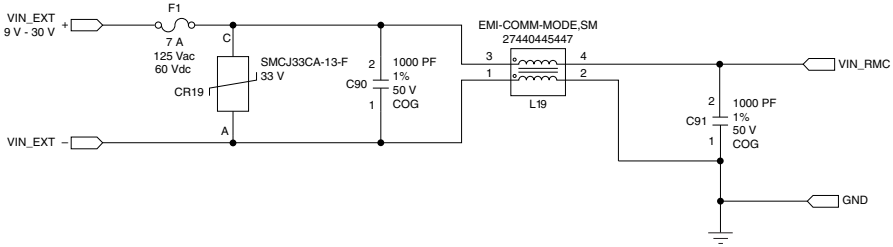
**Table 5.** Power Rails Signal Definitions (Continued)

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| 5V C Series | 86<br>91 | O | 5 V | Signal-conditioned C Series DIO. |
| VIN_Filtered | 1<br>7<br>14<br>20 | I | — | 9 V to 30 V input to power the sbRIO device through the RMC connector rather than through the front panel connector. |

## VIN_Filtered Implementation on the RMC

The following figure shows a schematic design for the VIN_Filtered implementation on the RMC.

**Figure 1.** VIN_Filtered Reference Schematic




Connect a well-regulated voltage that falls in the range of 9 V to 30 V to the VIN_Filtered pins to power up the board.

Include a common mode choke in the design before connecting the voltage rails to the RMC connector. Place a transient voltage suppressor before the common choke. NI recommends including a fuse in your design to protect the voltage transient suppressor.

### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 6.** Power Rails Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| TVS Selection | The recommended part is SMCJ33CA-13-F from Diodes. Any TVS with reverse standoff voltage and breakdown voltage of more than 30 V can be designed in. |
| Common Mode Choke | The recommended part is 2744045447 from Fair-Rite. Alternatively, use a common mode choke that matches the performance of this part in terms of the DC and AC impedance. |
| Capacitor | 1000 pf is the recommended value of the decoupling input and output capacitor. The recommended part is a ceramic COG. |
| Fuse | The recommended part is TR1/6125TD7-R from Eaton if the only load after the fuse is the VIN_RMC input pin to the sbRIO device. Use a 7 A fuse to provide sufficient margin and prevent false blows due to temperature and process variations. If you choose to connect other loads after the fuse, you must account for the extra current drawn by that load when selecting a fuse. |

# Gigabit Ethernet (GBE)

The sbRIO device provides a secondary Gigabit Ethernet port (GBE) for use on an RMC.

## GBE Signal Definitions

The following table describes the GBE port pins and signals on the sbRIO device connector.

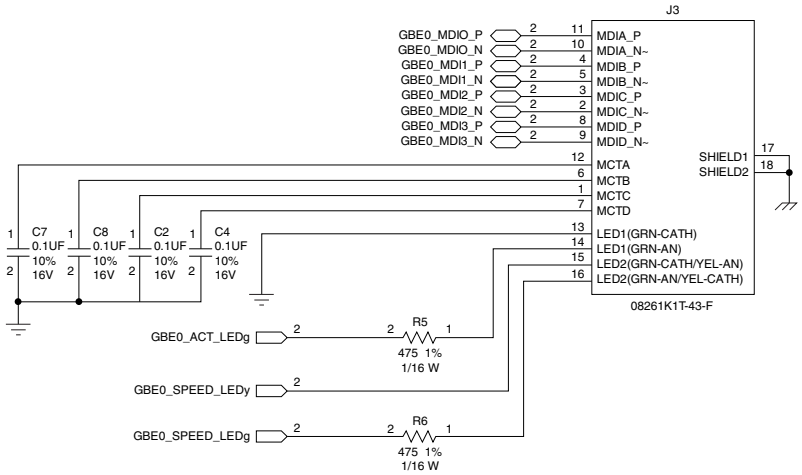
**Table 7.** GBE Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| GBE_MDI0+<br>GBE_MDI0-<br>GBE_MDI1+<br>GBE_MDI1-<br>GBE_MDI2+<br>GBE_MDI2-<br>GBE_MDI3+<br>GBE_MDI3- | 3<br>9<br>16<br>22<br>5<br>11<br>18<br>24 | I/O | Defined by Ethernet PHY specification | Pre-magnetic Gigabit Ethernet data pairs. |
| GBE_SPEED_LEDg<br>GBE_SPEED_LEDy | 37<br>31 | O | $LVTTL_{3.3V}$ | Speed LED signals. |
| GBE_ACT_LEDg | 32 | O | $LVTTL_{3.3V}$ | Activity/link LED signal. |

## GBE Implementation on the RMC

The following figure shows a schematic design for the GBE implementation on the RMC.

**Figure 2.** GBE Reference Schematic




## Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 8.** GBE Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| MDI data pairs | • The MDI data pairs are routed differentially and connected directly to the Ethernet connector.<br>• The Ethernet connector has the required Ethernet magnetics built into it. You may use discrete magnetics instead. |
| LED signals | • You can use the LED signals to directly drive connector LEDs.<br>• Size the current-limiting resistors to not exceed 8 mA drive current.<br>• Refer to the *Ethernet Speed LED Behavior* table of the *NI sbRIO-9607 User Manual* or *NI sbRIO-9627 User Manual* for information about Ethernet LED signal behavior. |

# Gigabit Ethernet Magnetic Requirements

The Ethernet PHY on the sbRIO device uses voltage-mode drivers for the MDI pairs, which greatly reduces the power that the magnetics consume and eliminates the need for a sensitive center tap power supply.

You must consider the following requirements for connecting center taps:

- Do not connect the center taps of the isolation transformer on the MDI pair side to any power source. Keep the center taps separate from each other.
- Connect each center tap through separate 0.1 µF capacitors to ground. The separation is required because the common-mode voltage on each MDI pair might be different.

The following table lists recommended magnetic characteristics.

**Table 9.** Recommended Magnetic Characteristics

| Parameter | Value | Test Condition |
|---|---|---|
| Turns ratio | 1 CT : 1 CT | — |
| Open-circuit inductance (minimum) | 350 µH | 100 mV, 100 kHz, 8 mA |
| Insertion loss (maximum) | 1.0 dB | 0 MHz to 100 MHz |
| HIPOT (minimum) | 1500 Vrms | — |

The following table describes the Gigabit Ethernet connector parts.

**Table 10.** Gigabit Ethernet Connector Parts

| Part | Manufacturer | Part Number |
|---|---|---|
| sbRIO-9607/sbRIO-9627 PHY | Micrel | KSZ9031RNX |
| RMC Gigabit Ethernet connector | Bel Stewart Magjack | 0826-1K1T-43-F |

Refer to the datasheet for the Micrel Ethernet PHY for more information about magnetic requirements.

## GBE Routing Considerations

NI recommends the following design practices for properly routing GBE signals on your RMC:

- Route MDI pairs differentially with 100 Ω differential trace impedance.
- Length-match the positive and negative signal for each MDI data pair to within 10 mils.
- Limit the MDI trace lengths on the RMC to 6.0 in. or less, which is the length at which Ethernet compliance was tested.

# USB Host/Device (USB)

The sbRIO device provides one USB 2.0-compliant ports for use on an RMC.

**Note** Your RMC design must provide the 5 V USB_VBUS power to USB Host ports and must limit the current supplied to each host port according to USB specifications.

## USB Host/Device Signal Definitions

The following table describes the USB Host/Device port pins and signals on the sbRIO device connector.

**Table 11.** USB Host/Device Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| USB_D+<br>USB_D- | 29<br>35 | I/O | Defined by USB specification | Port for hi-speed differential USB. |
| USB_MODE | 34 | I | — | Connect to digital ground or leave disconnected to configure the USB port as Host.<br>Connect to +3.3V to configure the USB port as Device. |
| USB_CPEN | 33 | O | $LVTTL_{3.3V}$ | USB over-current protection enable. |
| USB_VBUS | 84 | I | 5 V tolerant voltage sense | USB VBUS input. Allows USB PHY to sense if VBUS is present on the connector. |

## Configuring the USB Mode

You can configure the USB interface to be a USB Host port or a USB Device port, as shown in the following table. This mode is set when the system boots and does not change dynamically.

**Note** USB On-The-Go (OTG) is not supported.

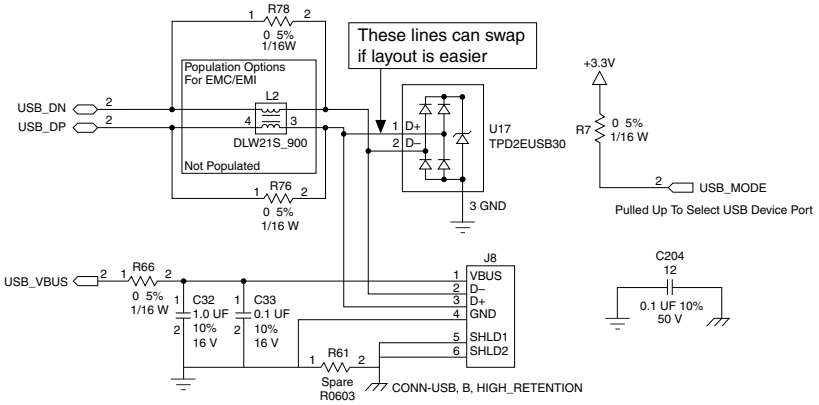
**Table 12.** Configuring the USB Mode

| Mode | How to Enable |
|---|---|
| USB Host | Connect the USB_MODE signal to digital ground or leave disconnected on your RMC. Refer to the *USB Host Implementation on the RMC* section for more information about the USB Host implementation on the RMC. |
| USB Device | Connect the USB_MODE signal to the +3.3V rail on your RMC. Refer to the *USB Device Implementation on the RMC* section for more information about the USB Device implementation on the RMC. |

## USB Device Implementation on the RMC

The following figure shows a schematic design for the USB Device implementation on the RMC.

**Figure 3.** USB Device Reference Schematic




### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

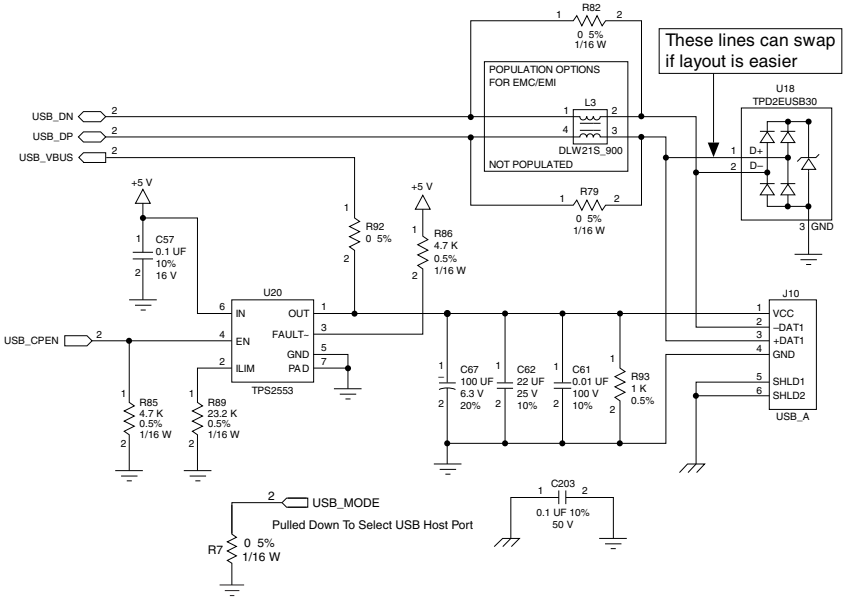
**Table 13.** USB Device Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| USB data pairs | • The USB_D+ and USB_D- data pair is routed differentially to the USB connector.<br>• On the RMC, the L2 common-mode choke is not populated, but you can populate it in your design to help with conducted immunity or emissions.<br>• If you choose to populate L2, remove R76 and R78 from your design.<br>• If your design does not include a common-mode choke, you can route the USB pair directly from the USB connector to the sbRIO device connector.<br>• U17 provides ESD protection to the USB data pair and should be placed close to the USB connector. |
| USB_MODE | The USB_MODE signal is connected directly to 3.3 V to select USB Device functionality. |
| USB_CPEN | Leave the USB_CPEN signal disconnected for a USB Device port. |
| USB_VBUS | • For the USB Device port to function properly, connect the USB_VBUS signal to the VBUS pin on the USB connector.<br>• This is a low-current, voltage-sense connection.<br>• In layout, you can treat this connection as a data signal.<br>• Connect the USB_VBUS signal directly to the VBUS pin on the USB connector or connect through R66, which must be a 0 Ω jumper. Overvoltage protection is included on the sbRIO device. |

## USB Host Implementation on the RMC

The following figure shows a schematic design for the USB Host implementation on the RMC.

**Figure 4.** USB Host Reference Schematic




## Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 14.** USB Host Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| USB data pairs | • The USB_D+ and USB_D- data pair is routed differentially to the USB connector.<br>• The L3 common-mode choke is not populated, but you can populate it in your design to help with conducted immunity or emissions.<br>• If you choose to populate L3, remove R79 and R82 from your design.<br>• If your design does not include a common-mode choke, you can route the USB pair directly from the USB connector to the sbRIO device connector.<br>• U18 provides ESD protection to the USB data pair and should be placed close to the USB connector. |
| USB_MODE | The USB_MODE signal is connected directly to 0 V to select USB Host functionality. |

**Table 14.** USB Host Reference Schematic Design Considerations (Continued)

| Consideration | Notes |
|---|---|
| USB_CPEN | Connect the USB_CPEN signal to the enable of the VBUS current limit switch (U20) so that the sbRIO device can power-cycle USB devices when the processor is reset. |
| USB_VBUS | • For the USB Host port to function properly, connect the USB_VBUS signal to the VBUS pin on the USB connector.<br>• This is a low-current, voltage-sense connection.<br>• In layout, you can treat the trace after R92 going to the sbRIO device connector as a data signal.<br>• Connect the USB_VBUS signal directly to the VBUS pin on the USB connector or connect through R92, which must be a 0 Ω jumper. Overvoltage protection is included on the sbRIO device.<br>• The RMC must provide 5 V VBUS power for the USB Host port.<br>• A current limit switch is required between the 5 V rail and the USB connector.<br>• U20 is the current limiter.<br>• NI recommends that you provide 100 µF capacitance on the VBUS rail. |

## Supporting Onboard USB Devices

When you implement a USB device directly on your RMC, you can connect the device to a USB Host port from the sbRIO device. For this case, use the following design guidelines:

- You can connect the USB data pair directly to a USB device on your RMC.
- A current limiter is not required.
- Use the RST# signal to reset the USB device when the sbRIO device is in reset.
- Tie the USB_VBUS signal to 5 V.

## USB Routing Considerations

NI recommends the following design practices for properly routing USB signals on your RMC:

- Route the USB_D+ and USB_D- signals as differential pairs with 90 Ω differential impedance.
- Length-match the positive and negative signal for each USB data pair to within 10 mils.
- Limit the USB_D+ and USB_D- trace lengths on the RMC to 8.0 in. or less, which is the length at which USB compliance was tested.

# C Series (SLOT 1, SLOT 2)

The sbRIO device provides two C Series slots for use on an RMC, which is Slot 1 and Slot 2.

## C Series Signal Definitions

The following table describes the C Series slot pins and signals on the sbRIO device connector.

**Table 15.** C Series Signal Definitions

| Signal Name | Dedicated Pin # | | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|---|
| | Slot 1 | Slot 2 | | | |
| ID_SELECT#[x] | 40 | 63 | I/O | $LVTTL_{3.3V}$ | Signal-conditioned C Series DIO. |
| OSCLK_DIO0[x] | 58 | 76 | | $LVTTL_{5V}$ | |
| TRIG_DIO1[x] | 64 | 82 | | tolerant input | |
| DONE#_DIO2[x] | 50 | 68 | | | |
| CVRT#_DIO3[x] | 46 | 69 | | | |
| SPIFUNC_DIO4[x] | 53 | 77 | | | |
| SPICS#_DIO5[x] | 55 | 73 | | | |
| MISO_DIO6]x] | 71 | 81 | | | |
| MOSI_DIO7[x] | 56 | 74 | | | |
| SPI_CLK[x] | 61 | 79 | | | |
| SLEEP[x] | 45 | 51 | O | 5 V | |
| 5V C Series | 86 | 91 | | | |

## C Series Implementation on the RMC

The following figures show schematic designs for the C Series implementation on the RMC.

**Figure 5.** C Series with Current Limiter Reference Schematic

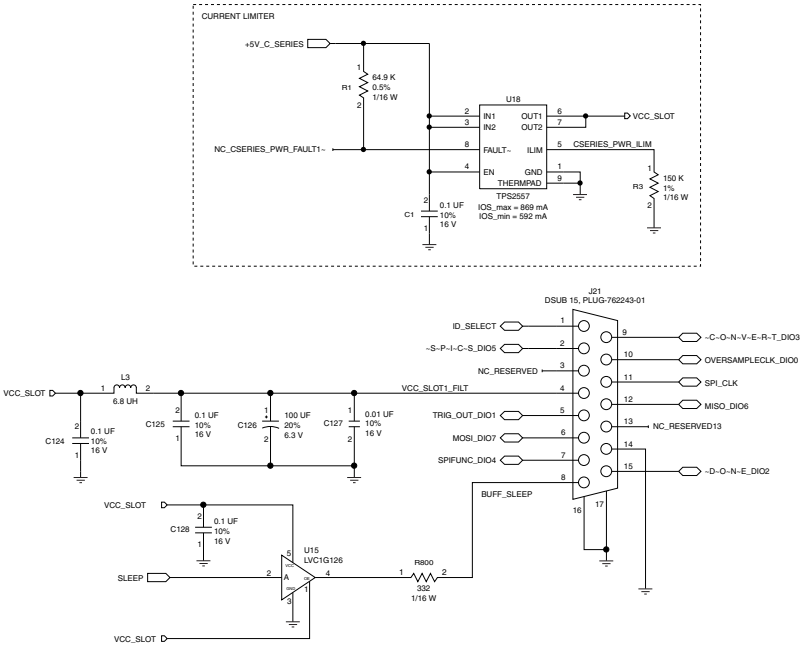
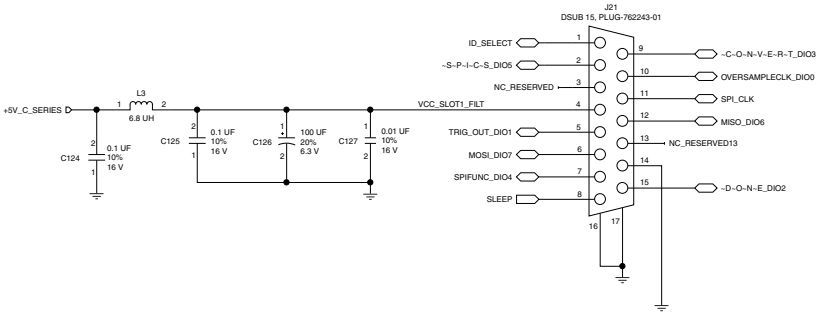



**Figure 6.** C Series without Current Limiter Reference Schematic




Use a current limiter to protect the PI inductor from overcurrenting in a fault condition and prevent the 5 V pin from accidentally shorting to either GND or CHSY. This protection is beneficial in environments where hot-plugging C Series modules are used.

## Reference Schematic Design Considerations

The following table lists design considerations for the schematics shown in the previous figures.

**Table 16.** C Series Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| Current limiter U18 | If a current limiter is used, you must re-buffer the sleep signal to the DSUB connector. If a current limiter is not used, you can connect the sleep signal directly to the DSUB connector by removing U15 in the schematic. The buffer prevents the sleep signal from being driven to the C Series module in an overcurrent condition. |
| Inductor L3 | Power PI Filter specifications:<br>• Value: 6.8 µH ±20%<br>• ESR: <200 mΩ<br>• Rated Current: >=400 mA |
| Capacitor C126 | Power PI Filter specifications:<br>• Value: 100 µF ±20%<br>• ESR: <100 mΩ |

## C Series Routing Considerations

NI recommends the following design practices for properly routing C Series signals on your RMC[3]:

- Route the signals with 55 Ω ±10% impedance.
- Length-match each signal to within 250 mils.
- Limit each signal trace length on the RMC to 10.0 in. or less, which is the length from the RMC SEARAY connector to DSUB connector.
- Maintain at minimum a 3 × H line spacing between single-ended traces, where H is the distance in the board stack-up from the trace to its reference plane.

# RTC Battery (VBAT)

The RMC contains a lithium cell battery that maintains the real-time clock (RTC) on the sbRIO device when the sbRIO device is powered off. A slight drain on the battery occurs when power is not applied to the sbRIO device. The following table lists the VBAT power specifications.

[3] SLEEP lines and 5V_C SERIES are exempted from these requirements.

**Table 17.** VBAT Power Specifications

| Specification | Minimum | Typical | Maximum |
|---|---|---|---|
| VBAT input voltage | 2.875 V | 3.0 V | 5.5 V |
| sbRIO device powered VBAT current | — | 25 nA | 100 nA |
| sbRIO device unpowered VBAT current | — | 2.6 µA average | 4.2 µA average |

If the battery is dead, and if no voltage has been applied to the VBAT pins, the system still starts but the system clock resets to the UNIX epoch date and time.

## VBAT Signal Definitions

The following table describes the VBAT pins and signals on the sbRIO device connector.

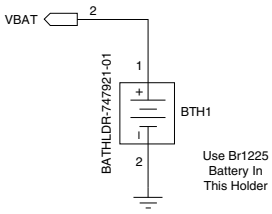
**Table 18.** VBAT Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| VBAT | 236 | I | Power rail | RTC battery input that provides backup power to the RTC to maintain absolute time. |

## VBAT Implementation on the RMC

The following figure shows a schematic design for the VBAT implementation on the RMC.

**Figure 7.** VBAT Reference Schematic




### Reference Schematic Design Considerations

You can directly connect the battery to VBAT. The sbRIO device already provides a current-limiting resistor and reverse-voltage protection.

# Resets

The sbRIO device provides signals for implementing a reset button on an RMC and indicating that the sbRIO device is in reset.

## Reset Signal Definitions

The following table describes the Reset pins and signals on the sbRIO device connector.

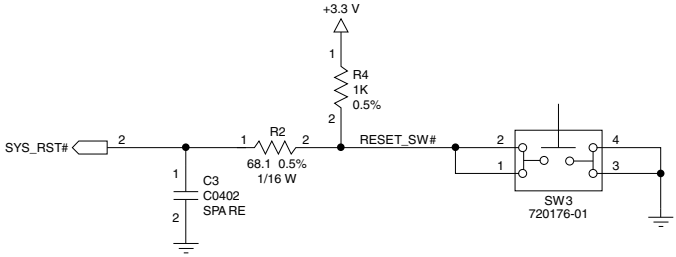
**Table 19.** Reset Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| RST# | 38 | O | $LVTTL_{3.3V}$ | Reset that indicates that main power is not adequate or that the sbRIO device is in reset. Asserted low. |
| SYS_RST# | 43 | I | $LVTTL_{3.3V}$ | System reset that puts the sbRIO device in reset. Asserted low.<br>Asserting this signal causes the RST# signal to also assert.<br>You can also assert this signal to put the sbRIO device into safe mode or reset IP address settings. |

## Reset Implementation on the RMC

The following figure shows a schematic design for the Reset implementation on the RMC.

**Figure 8.** Reset Reference Schematic




Refer to the *SYS RST#* and *RMC RST#* sections of the *NI sbRIO-9607 User Manual* or *NI sbRIO-9627 User Manual* for more information about the behavior of the Reset signals.

### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 20.** Reset Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| Series termination | When SYS_RST# is driven, you must place a series termination resistor at the driver. When the driver is a mechanical switch, placing series termination is especially important due to the low output impedance of the switch. |

# FPGA Config

The sbRIO device provides an FPGA Config signal to indicate when the FPGA is configured.

## FPGA Config Signal Definitions

The following table describes the FPGA Config pins and signals on the sbRIO device connector.

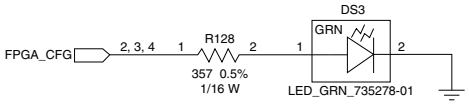
**Table 21.** FPGA Config Signal Definitions

| Signal Name | Dedicated Pin # | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|---|
| FPGA_CONF | 239 | O | Refer to the *NI sbRIO-9607 User Manual* or *NI sbRIO-9627 User Manual* for more information about the behavior of this signal. | FPGA Config Asserts when the FPGA is configured. Asserted high when the FPGA has been programmed. |

## FPGA Config Implementation on the RMC

The following figure shows a schematic design for the FPGA Config implementation on the RMC.

**Figure 9.** FPGA Config Reference Schematic




Refer to the *FPGA_CONF* section of the *NI sbRIO-9607 User Manual* or *NI sbRIO-9627 User Manual* for more information about the behavior of the FPGA Config signal.

# User-Defined FPGA Signals

The sbRIO device connector provides several FPGA pins that you can configure for purposes specific to your application. In addition to FPGA Digital I/O (DIO), you can use these pins to implement the following run-time peripheral interfaces:

- RS-232
- RS-485
- CAN
- SDIO

Refer to the specific sections in this chapter for more information about how the RMC implements each signal.

**Note** To read or write to this I/O from a LabVIEW project, you must use the sbRIO CLIP Generator application to create a socketed component-level IP (CLIP) that defines the I/O configuration of the sbRIO device to use in your application. Refer to the *NI Single-Board RIO CLIP Generator Help* for more information about creating a CLIP.

## User-Defined FPGA Signal Definitions

The following table describes the 96 user-defined FPGA pins and signals on the sbRIO device connector.

**Table 22.** User-Defined FPGA Signal Definitions

| Signal Name | Direction (from Host System) | I/O Standard | Description |
|---|---|---|---|
| DIO [0..95] | I/O | $LVTTL_{3.3V}$ | Pins for connecting directly to the FPGA through a series resistor and for enabling serial, CAN, or SDHC peripherals on an RMC. |

## Additional RS-232

You can use any FPGA pins to implement additional RS-232 ports.

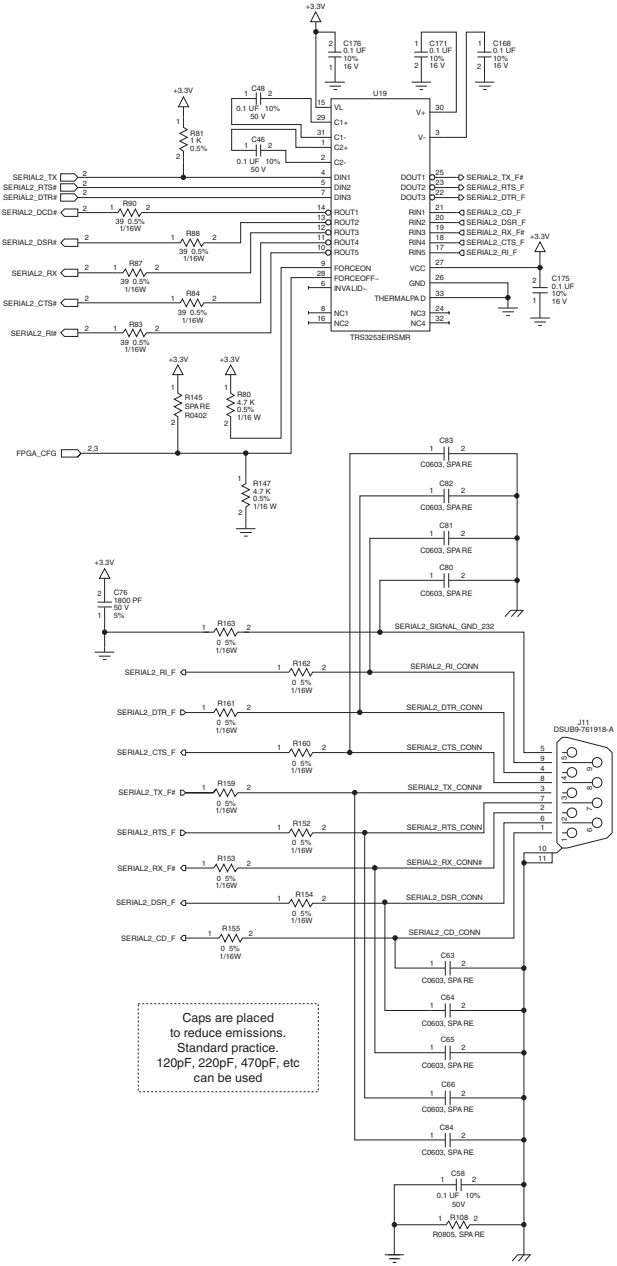
Number of interfaces:

- sbRIO-9607—4 (Serial2, Serial3, Serial4, Serial5)
- sbRIO-9627—4 (Serial4, Serial5, Serial6, Serial7)

### RS-232 Reference Schematic

The following figure shows a schematic design for the RS-232 implementation on the RMC.

**Figure 10.** RS-232 Reference Schematic



### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 23.** RS-232 Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| Interface | The RMC reference schematic demonstrates how to use the Serial2 interface to implement a null-modem RS-232 serial port. |
| Serial transceiver | U19 is the RS-232 serial transceiver that converts between RS-232 and LVTTL signal levels. To minimize the impact of higher voltage signals on your RMC, place the serial transceiver near the RS-232 connector. |
| Series termination | • R83, R84, R87, R88, and R90 are the series termination for Serial2. Use series termination at the serial transceiver on all signals being driven to the sbRIO device.<br>• All FPGA DIO signals on the sbRIO device include series termination. |
| FPGA | All serial port signals pass through the FPGA on the sbRIO device. The FPGA_CONF signal is used to disable the serial transceiver when the FPGA is not configured. Disabling the transceiver in this way prevents any unwanted glitches on the RS-232 port. |

# Additional RS-485

You can use any FPGA pins to implement additional RS-485 ports.

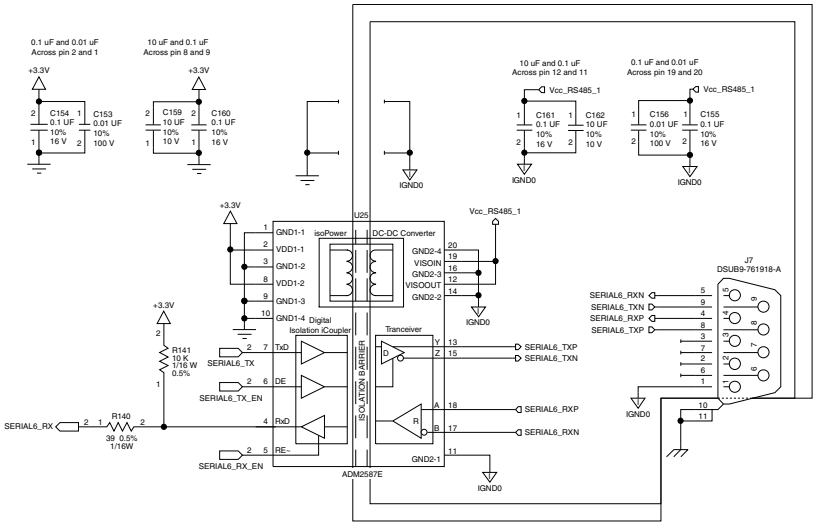
Number of interfaces:

- sbRIO-9607—2 (Serial6, Serial7)
- sbRIO-9627—2 (Serial8, Serial9)

## RS-485 Reference Schematic

The following figure shows a schematic design for the RS-485 implementation on the RMC.

**Figure 11.** RS-485 Reference Schematic




## Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 24.** RS-485 Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| Interface | The RMC demonstrates how to use the Serial6 interface to implement a null-modem RS-485 serial port. |
| Serial transceiver | U25 is the RS-485 serial transceiver that converts between RS-485 and LVTTL signal levels. This transceiver provides functional isolation of the RS-485 signals to prevent ground loops from affecting the RS-485 signals. |
| Series termination | • R140 is the series termination for Serial6. Use series termination at the serial transceiver on all signals being driven to the sbRIO device.<br>• All FPGA DIO signals on the sbRIO device include series termination. |

# RS-485 Layout Considerations

Pay close attention to how the ground planes are arranged under the isolated RS-485 transceiver. Isolated and non-isolated ground planes overlap across layers to provide some

capacitance between the grounds and help with EMC. Refer to the datasheet for the RS-485 transceiver for more information.

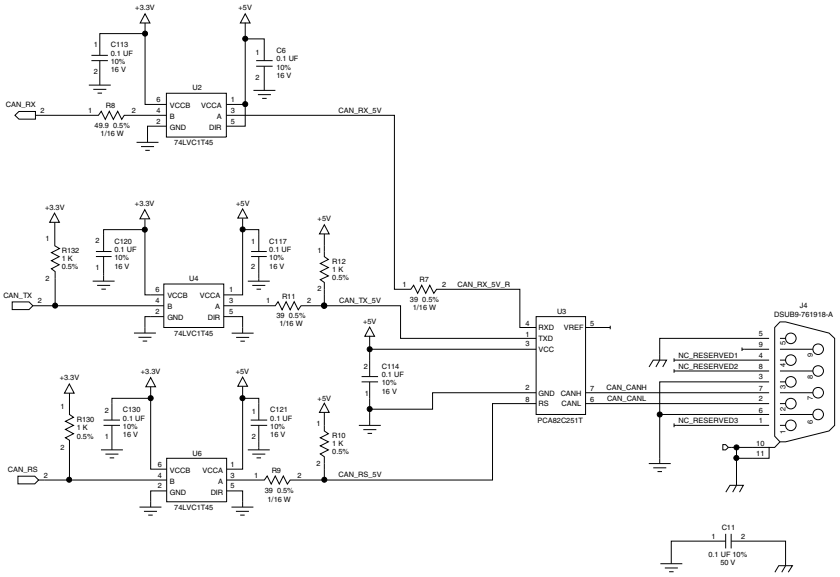
# CAN

You can use any FPGA pins to implement the single CAN (CAN1) interface port available through the RMC.

## CAN Reference Schematic

The following figure shows a schematic design for the CAN implementation[4] on the RMC.

**Figure 12.** CAN Reference Schematic




### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

[4] The NXP PCA82C25IT CAN transceiver requires 5 V logic levels. The RMC uses external discrete buffers to translate 3.3 V FPGA lines to 5 V logic levels.

**Table 25.** CAN Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| CAN_RX,<br>CAN_TX, and<br>CAN_RS | • The recommended CAN transceiver requires 5 V I/O.<br>• U2, U4, and U6 provide level translation between the 3.3 V I/O on the sbRIO device and the 5 V I/O on the transceiver. Use caution when implementing this level translation.<br>• The TXD and RS inputs of the CAN transceiver must remain high during power-down and power-up of the sbRIO device and RMC. This prevents glitches on the CAN bus that might disrupt communication between other devices on the bus. The level translator IC in this schematic prevents these glitches.<br>• The level translator output remains at high impedance until both of its power supply rails are powered to allow the 5 V power supply to power-up before the 3.3 V power supply.<br>• All signals have series termination at the outputs to prevent overshoot or undershoot at the receivers.<br>• All FPGA DIO signals on the sbRIO device include series termination. |
| CAN_CANH<br>and<br>CAN_CANL | • Route these signals differentially with a 120 Ω differential trace impedance.<br>• Minimize the overall length of the traces so that you can place termination resistors in the CAN cabling as close as possible to the CAN transceiver.<br>• Depending on your design requirements, you can also place the CAN termination resistor on the RMC. |

## Termination Resistors for CAN Cables

The termination resistors should match the nominal impedance of the CAN cable and therefore comply with the values in the following table.

**Table 26.** Termination Resistor Specification

| Characteristic | Value | Condition |
|---|---|---|
| Termination resistor | 100 Ω minimum<br>120 Ω nominal<br>130 Ω maximum | Minimum power dissipation: 220 mW |

# SDIO

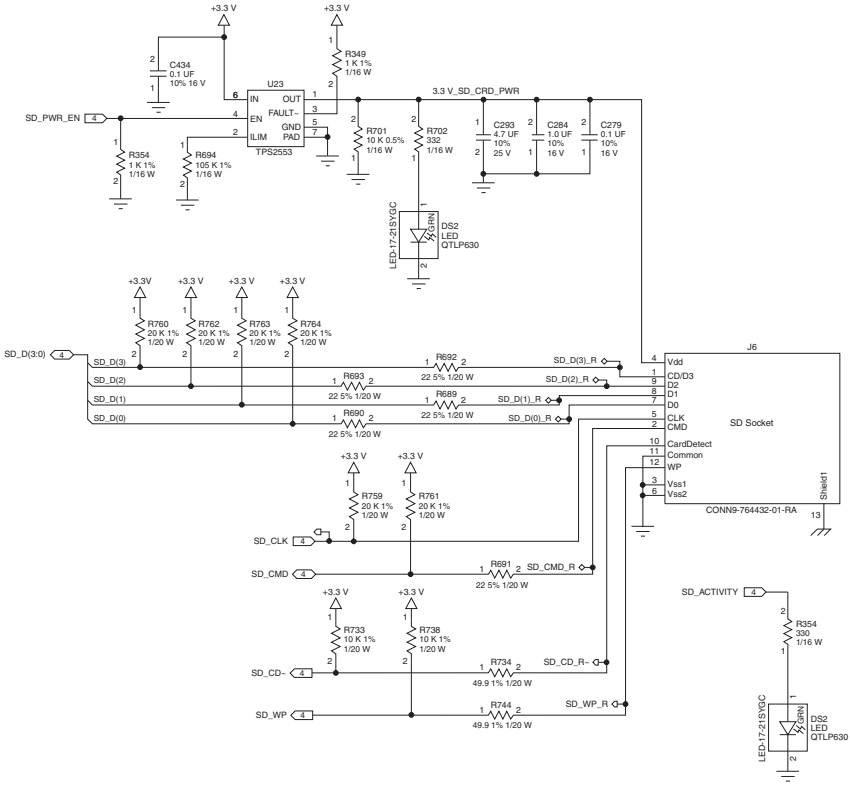
The sbRIO device provides a Secure Digital (SD) Card interface for use on an RMC. This interface supports SD and SDHC cards. You can implement this interface with standard SD or microSD card connectors. The maximum supported SDHC card capacity is 32 GB.

You can use any FPGA pins to implement a SDIO interface.

## SD Reference Schematic

The following figure shows a schematic design for the SD implementation on the RMC.

**Figure 13.** SD Reference Schematic




### Reference Schematic Design Considerations

The following table lists design considerations for the schematic shown in the previous figure.

**Table 27.** SD Reference Schematic Design Considerations

| Consideration | Notes |
|---|---|
| SD_CLK,<br>SD_CMD<br>SD_D0<br>SD_D1<br>SD_D2<br>SD_D3 | • You can route these signals directly from the sbRIO device to the SD connector.<br>• Each of these signals requires series termination near its driver. The sbRIO device provides series termination near the Xilinx Zynq SoC to prevent overshoot on the SD card when the sbRIO device drives these signals. The bi-directional signals also require series termination at the SD card socket.<br>• Use series termination at the SD connector for the SD_CMD and SD_D0 through SD_D3 signals to prevent overshoot on the sbRIO device when the SD card drives these signals.<br>• Each of these signals requires a pull-up resistor to 3.3 V to ensure the voltage level stays at 3.3 V when the FPGA is not configured. This configuration is required according to the SDIO specification. |
| SD_CD# | • The SD_CD# signal is connected to the mechanical card-detect switch in the SD connector.<br>• When a card is inserted, the card-detect pin on the SD connector is shorted to ground.<br>• Because this is a mechanical switch with low output impedance, you must place a series termination resistor (R734) at the SD connector.<br>• You must have a card-detect switch to properly support hot-swapping cards. If you do not need to support hot-swapping cards, you can use an SD connector without a card-detect switch. In this case, tie the SD_CD# signal to ground so that the sbRIO device attempts to initialize a card on boot.<br>• Each of these signals requires a pull-up resistor (R733) to 3.3 V to ensure the voltage level stays at 3.3 V when the switch is not activated. |

**Table 27.** SD Reference Schematic Design Considerations (Continued)

| Consideration | Notes |
|---|---|
| SD_WP | • When the SD_WP signal is asserted high, the sbRIO device will not write to the SD card.<br>• Standard-size SD card connectors provide a mechanical write-protect switch that you can connect to the SD_WP signal. The switch detects the position of the lock slide on the SD card.<br>• Because this is a mechanical switch with low output impedance, you must place a series termination resistor (R744) at the SD connector.<br>• If you are using a microSD connector or do not have a write-protect switch, you can tie the SD_WP signal to ground in order to disable write protection and allow changes to the SD card.<br>• Each of these signals requires a pull-up resistor (R738) to 3.3 V to ensure the voltage level stays at 3.3 V when the switch is not activated. |
| SD_PWR_EN | • Use the SD_PWR_EN signal to gate power to the SD connector.<br>• U23 acts as a power switch and current limiter for the SD interface. SDHC cards must not draw more than 200 mA.<br>• The SD_PWR_EN signal controls when power is going to the SD card.<br>• The SD_PWR_EN signal asserts high when a card is detected using the SD_CD# signal. The SD_PWR_EN signal deasserts when a card is not present.<br>• Use a pull-down resistor (R354) to keep the SD_PWR_EN signal low when the FPGA is not configured. |

## SD Routing Considerations

NI recommends the following design practices for properly routing SD signals on your RMC:

- Length-match the SD_CMD and SD_D0 through SD_D3 signals to within ±250 mils of SD_CLK.
- Limit the trace length of the SD_CLK, SD_CMD, and SD_D0 through SD_D3 signals on the RMC to 15.0 in. or less.

# RMC PCB Layout Guidelines

Use the guidelines in this section to help you arrange the I/O signals you implement in your RMC.

# Impedance-Controlled Signaling

Use the following guidelines for implementing impedance for all I/O signals:

- All signals connected to the sbRIO device must use impedance-controlled traces. Refer to the sections of this document listed in the following table for information about impedance requirements.

**Table 28.** Impedance Requirements Resources

| Impedance Requirement | Resource |
|---|---|
| General requirements for single-ended signals | *Single-Ended Signal Best Practices* section of this document |
| General requirements for differential signals | *Differential Signal Best Practices* section of this document |
| Signal-specific requirements | Signal-specific sections in *Fixed Behavior Signals* or *User-Defined FPGA Signals* |

- Trace geometry to meet impedance requirements vary depending on your specific RMC PCB stack-up. Collaborate with your vendor to match impedance requirements, stack-up, and trace geometry appropriate for your application.
- To properly maintain trace impedance and avoid discontinuities, you cannot route traces over gaps in the reference plane. Use stitching vias and capacitors when appropriate near layer changes to provide a transient return path between reference planes.

# Single-Ended Signal Best Practices

Use the following guidelines for implementing single-ended I/O signals:

- Route all single-ended signals that are implemented on your RMC and connected to the sbRIO device with 55 Ω characteristic trace impedance.
- Maintain the following line spacing between single-ended traces, where H is the distance in the board stack-up from the trace to its reference plane:
  - 3 × H for C Series signals
  - 2 × H for all other signals
- Series termination resistors for FPGA DIO signals are included on the sbRIO device. Refer to the FPGA DIO section of the sbRIO device user manual on *ni.com/manuals* for more information.

## Differential Signal Best Practices

Use the following guidelines for implementing differential I/O signals:

- Route USB differential pair signals that are implemented on your RMC and connected to the sbRIO device with 100 Ω differential trace impedance.
- Route Ethernet MDI*x* differential pair signals that are implemented on your RMC and connected to the sbRIO device with 90 Ω differential trace impedance.
- Maintain at minimum a 3 × H spacing between differential pairs and any other copper features on the same layer, where H is the distance in the board stack-up from the trace to its reference plane.

## Ground Plane Recommendations

You must include ground planes on your RMC. All GND pins on the RMC connector of the sbRIO device must connect to the RMC ground planes.

## Fanout and Layout Options

Refer to Samtec SEARAY documentation for information about possible fanout and layout options with various layer count RMCs.

# Mechanical Considerations

Power dissipated on the RMC will affect and be affected by the power dissipated on the sbRIO device. You must provide serious consideration to the thermal performance of both the RMC and sbRIO device to ensure that your applications meets component specifications. Refer to the sbRIO device user manual and specifications on *ni.com/manuals* for more information about validating the thermal performance of the sbRIO device. The following recommendations may increase the thermal performance of the system:

- Spread high-power dissipating components across the surface of the printed circuit board rather than placing them in close proximity to each other.
- Place high-power dissipating components on the side of the board opposite the RMC connector.
- Minimize the amount of dissipation by the RMC in the area directly underneath the sbRIO device as this will greatly influence the sbRIO device secondary side local ambient temperature.
- Design and validate a thermal solution for the high-power dissipating components of your RMC.

When deploying in environments that could experience high levels of shock or vibration, the following recommendations may increase the robustness of the system:

- Use a printed circuit board at least 2 mm (0.79 in.) thick.
- Use positive locking connectors with thru-hole technology and the greatest practical amount of gold plating on contacts.
- Design mechanical features for strain relief and retention of connectors and cables.

# Selecting an Appropriate Mating Connector

The J1 connector on the sbRIO device is a Samtec SEAF-40-06.5-S-06-2-A-K-TR 240-pin, 6 x 40 position, SEARAY open-pin-field-array connector. To interface with the J1 connector, your RMC design must implement a mating connector that is compatible with the Samtec SEAF series. The following table lists compatible mating connectors.

**Table 29.** Connector and Compatible Mating Connectors

| Connector | Manufacturer, Part Number |
|---|---|
| J1 connector | Samtec SEAF-40-06.5-S-06-2-A-K-TR |
| Recommended mating connector[5] | Samtec SEAM-40-03.0-S-06-2-A-K-TR |

# Selecting Appropriate Standoffs

The Samtec SEAM series connectors are available in multiple heights. The height of the mating connector you select helps determine the height of the standoffs you need.

To prevent over-insertion, the SEARAY connector design requires that standoffs never be less than the stack height. Because standard nominal tolerances might result in a standoff being shorter than the stack height, NI requires that you use standoffs that are 0.15 mm (0.006 in.) taller than the combined height of the J1 connector on the NI sbRIO device and the mating SEARAY connector. Therefore, to determine the required standoff height, you must add the heights of the mated connectors plus an additional 0.15 mm (0.006 in.). Refer to Samtec documentation for more information about SEARAY standoff requirements.

The following table provides an example standoff height calculation using a Samtec SEAM-40-03.0-S-06-2-A-K-TR mating connector.

**Table 30.** Example Connector Configuration and Calculated Standoff Height

| Component | Manufacturer, Part Number | Height |
|---|---|---|
| J1 connector | Samtec SEAF-40-06.5-S-06-2-A-K-TR | 6.50 mm (0.256 in.) |
| Mating connector | Samtec SEAM-40-03.0-S-06-2-A-K-TR | 3.00 mm (0.118 in.) |
| Required additional standoff height | — | 0.15 mm (0.006 in.) |
| Total calculated standoff height | — | 9.65 mm (0.380 in.) |

[5] Compatible connectors are available in multiple stack height and termination options.

## NI Custom Standoffs

NI offers a custom standoff that is an exact fit with the recommended or other compatible 9.5 mm (0.374 in.) stack height mating connectors listed in the table on *Selecting an Appropriate Mating Connector*. This custom M3 × 9.65 mm (0.380 in.) standoff is made from 4.5 mm (0.177 in.) stainless steel hex stock and includes a nylon threadlock patch. The external threads extend 4.78 mm (0.188 in.) and the internal threads are 5 mm (0.197 in.) deep. The standoff is available from NI in quantities of 12 by ordering part number 153166-12.

NI recommends that you use stainless steel fasteners for good corrosion resistance and strength. Tighten M3 fasteners to a torque of 0.76 N · m (6.70 lb · in), unless otherwise noted or required by your specific design constraints.

# Worldwide Support and Services

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